

disclosure, will recognize variations and modifications of the disclosed embodiments, which none the less fall within the spirit and scope of the appended claims.

We claim:

1 1. A processor comprising:
2 a protected execution unit to process instructions;
3 a check unit to detect an error associated with processed instructions; and
4 a replay queue to issue instructions to the protected execution unit for processing,
5 track the issued instructions, and reissue selected issued instructions when the check unit
6 detects an error.

1 2. The processor of claim 1, wherein instructions are flushed from the execution unit when
2 the check unit indicates an error.

1 3. The processor of claim 1, wherein the replay queue includes first and second pointers to
2 indicate a next instruction to issue and a next instruction to retire.

1 4. The processor of claim 3, wherein the replay queue adjusts the first pointer and second
2 pointers to reissue instructions to the execution unit beginning with an instruction that generated
3 the result mismatch.

1 5. The processor of claim 4, wherein the protected execution unit comprises first and second
2 execution units to process instructions in lock step and the replay queue comprises first and
3 second replay queues to provide instructions to the first and second execution units, respectively.

1 6. The processor of claim 1, wherein the execution units operate in lock step when the
2 processor is in a high reliability mode and the execution units independently when the processor
3 is in a high performance mode.

1 7. The processor of claim 1, wherein the processor implements a recovery algorithm if an
2 instruction that triggers a replay generates a mismatch when it is replayed.

1 8. A method for executing instructions with high reliability, comprising:
2 storing an instruction temporarily in a replay buffer;
3 issuing the instruction to a protected execution unit;
4 checking results generated by the instruction in the protected execution unit; and
5 reissuing the instruction to the protected execution unit if an error is indicated.

1 9. The method of claim 8, wherein issuing the instruction comprises:
2 staging the instruction to the protected execution unit; and
3 adjusting a first flag in the buffer to indicate the instruction has been issued.

1 10. The method of claim 8, wherein adjusting the first flag comprises setting a first pointer to
2 indicate a buffer slot in which the issued instruction is stored.

1 11. The method of claim 10, further comprising setting a second pointer to indicate a buffer
2 slot in which a next instruction to retire is stored.

1 12. The method of claim 11, wherein reissuing the instruction comprises copying the second
2 flag to the first flag.

1 13. The method of claim 8, further comprising retiring the instruction when no error is
2 indicated.

1 14. The method of claim 13, wherein retiring the instruction comprises:
2 adjusting a second pointer to indicate the instruction has retired; and
3 updating an architectural state data with the result generated by the instruction.

1 16. A computer system comprising:
2 a processor that includes:
3 a protected execution unit to execute instructions in a manner that
4 facilitates soft error detection;
5 a check unit to monitor the protected execution unit and to generate a
6 signal when an error is indicated;

7 a replay unit to provide instructions to the protected execution unit, track
8 the instructions until they are retired, and replay selected instructions when the
9 check unit indicates an error; and
10 a storage structure to provide a recovery algorithm to the processor when replay
11 of selected instructions does not eliminate the mismatch.

1 16. The computer system of claim 15, wherein the replay unit includes first and second
2 pointers to indicate a next instruction to issue and a next instruction to retire, respectively.

1 17. The computer system of claim 16, wherein the execution units are flushed prior to the
2 replay when an error is indicated.

1 18. The system of claim 17, wherein the replay unit and the execution units are flushed prior
2 to implementing the recovery routine.

1 19. The computer system of claim 16, wherein the storage structure is a non-volatile memory
2 structure.

1 20. The computer system of claim 15, wherein the protected execution unit comprises first
2 and second execution units and the replay unit provides identical instructions to the first and
3 second execution units.

1 21. A processor comprising:
2 first and second execution cores to process identical instructions in lock step, each
3 execution core including a replay unit to track instructions that have yet to retire.
4 a check unit to compare instructions results generated by the execution cores and
5 to trigger the replay unit to re-steer the first and second execution cores to an instruction
6 when the instruction results generate a mismatch.

1 22. The processor of claim 21, wherein each replay unit includes buffer slots to store
2 instructions for execution and first and second pointers to indicate a next instruction to issue and
3 a next instruction to retire, respectively.

1 23. The processor of claim 22, wherein each replay unit copies the second pointer to the first
2 pointer when the instruction results generate a mismatch.

1 24. The processor of claim 23, wherein the check unit signals an instruction flush when a
2 mismatch is detected.